In the Claims:

1. (Cancelled).

2. (Cancelled).

3. (Cancelled).

4. (Cancelled).

5. (New) A software driven emulation engine for verifying functionality of logic designs comprising:

at least one module, said module comprising a plurality of processors that execute logic gate functions from a logic design, said processors organized into a plurality of clusters such that each of said plurality of clusters comprise a subset of said plurality of processors, each of said processors in each of said clusters accessing a data memory within each of said clusters;

a time division multiplexer associated with each of said clusters coupling a set of read ports of said data memory to a set of read addresses of one processor of said cluster during one read cycle of said data memory and coupling said set of read ports of said data memory to a set of read addresses of another processor of said cluster during the next read cycle of said data memory.

6. (Original) A software driven emulation engine as in claim 5 wherein said data memory operating clock rate for read operations is twice the operating clock rate of said module.

7. (New) A software driven emulation engine for verifying functionality of logic designs comprising:

at least one module, said module including a plurality of clusters wherein each of said clusters comprise a plurality of processors that execute logic gate functions from a logic design, each of said processors of each of said clusters accessing a data memory within each of said clusters;

a first time division multiplexer associated with each of said clusters that couples a first set of read ports of said data memory to a set of read addresses of a first processor of said cluster during one read cycle of said data memory and coupling said first set of read ports of said data memory to a set of read addresses of a second processor in said cluster during the next read cycle of said data memory;

a second time division multiplexer associated with each of said clusters that couples a second set of read ports of said data memory to a set of read addresses of a third processor of said cluster during said one read cycle of said data memory and coupling said second set of read ports of a set of read addresses of a fourth processor in said cluster during said next read cycle of said data memory.

8. (Original) A software driven emulation engine as in claim 7 wherein said data memory operating clock rate for read operations is twice the operating clock rate of said module.

9. (New) A emulation engine for verifying functionality of logic designs comprising:

at least one module, said module comprising a plurality of clusters, said clusters each comprising a plurality of processors that that execute logic gate functions from a logic design, each of said processors within each of said clusters accessing a data memory within each of said clusters;

a time division multiplexer associated with each of said clusters that couples a set of read ports of said data memory to a set of read addresses of one processor within a first of said clusters during one read cycle of said data memory and coupling said set of read ports of said data memory to a set of read addresses of another processor within said first of said clusters during the next read cycle of said data memory.